## **CLAIMS**

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

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1. A method of forming a field effect transistor (FET) transistor, comprising
providing a substrate;
forming a layer on the substrate, the layer having a side surface;
forming an epitaxial channel on the side surface, the channel having a
first sidewall;
removing the layer for exposing a second sidewall of the channel;
forming source and drain regions coupled to ends of the first channel
and
forming a gate adjacent to at least one of the sidewalls of the channel

↑ 2. A field effect transistor (FET) comprising:

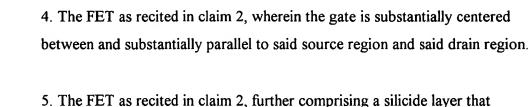
a substrate;

a source region and a drain region in the substrate, each of said source region and said drain region having a top, bottom and at least two side diffusion surfaces, the source and drain regions separated by an epitaxially grown channel region having a top, bottom and side channel surfaces substantially coplanar with corresponding ones of the diffusion surfaces;

a gate adjacent the top and the side channel surfaces and electrically insulated from the top and side channel surfaces; and

the gate comprising a planar top surface, the planar top surface having a contact for receiving a gate control voltage for controlling the FET.

3. The FET as recited in claim 2, wherein the source and drain have a contact for receiving a control voltage for controlling the FET.



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- 2 contacts a top surface of said gate.

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- 1 6. The FET as recited in claim 2, further comprising a dielectric layer that
- 2 contacts a first side end and a second side end of said gate.
- 1 7. The FET as recited in claim 2, further comprising a dielectric that contacts
- side surfaces of the channels. 2
- 1 8. The FET as recited in claims 2, where the gate is comprised of polysilicon.
- 1 9. The FET as recited in claim 2, wherein the channel is approximately one
- 2 fourth of a length of the FET.
- 10. The FET as recited in claim 2, further comprising a dielectric material in 1
- 2 the gate for electrically separating the gate into two electrically isolated
- 3 portions, each having a substantially coplanar top surface and a contact pad on
- each respective substantially coplanar top surface. 4
- 1 11. The FET as recited in claim 2, wherein said epitaxial channel is formed of
- 2 a combination of Group IV elements.
- 12. The FET as recited in claim 2, wherein said epitaxial channel is formed of 1
- 2 an alloy of silicon and a Group IV element.

13. The FET as recited in claim 2, wherein said epitaxial channel is formed of
an alloy of silicon and at least one of germanium and carbon.
14. A method for forming a double gated field effect transistor (FET),
comprising the steps of:
forming on a substrate a first and a second epitaxially grown channels;
etching areas within a silicon layer to form a source and a drain,
wherein a side surface of the source and the drain contact opposing end
surfaces of the first and second epitaxially grown channels; and
forming a gate that contacts a top surface and two side surfaces of the
first and second epitaxially grown channels and a top surface of the substrate.
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15. The method as recited in claim 14, wherein the forming step comprises the
steps of:
forming first and second silicon lines, each end of the silicon lines
contact an end of the source and the drain;
forming an etch stop layer on an exposed side surface of each of the
first and second silicon lines;
epitaxially growing first and second silicon layers on each etch stop
layer;
etching away the first and second silicon lines and etch stop layers;
filling areas surrounding the first and second epitaxially grown silicon
layers and between the source and the drain with an oxide fill;
etching a portion of the oxide fill to form an area that defines a gate,
wherein the area that defines the gate is substantially centered between and
substantially parallel to the source and the drain; and
depositing a material to form a gate.

16. The method as recited in claim 15, further comprising the steps of:

23. The method as recited in claim 14, wherein the gate material is polysilicon.

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